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EXAMINER	
LANDAU, MATTHEW C	

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2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,892	RHODES, HOWARD E.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-93* is/are pending in the application.

4a) Of the above claim(s) *11,12,23,30,44,53-84 and 90-93* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-22,24-29,31-43,45-52 and 85-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, Species IA in the reply filed on January 24, 2005 is acknowledged.

After reviewing the specification, it is clear that claim 23 reads on a non-elected species. According to the specification (paragraph [[0052]), the reset transistor has an increased gate length only in the 3 transistor embodiment (which corresponds to Species IB). Therefore, claims 11, 12, 23, 30, 44, 53-84, and 90-93 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention/species, there being no allowable generic or linking claim.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the single active area extension region and said halo implant region spaced away from a gate of said first transistor by a portion of a substrate supporting said first transistor (claim 8) while the halo implant region extends partially below the gate (claim 6) must be shown or the feature(s) canceled from the claim(s). Note that claim 8 depends from claim 6. No drawing shows the combination of features indicated by these claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet,

even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 22, 26, and 49 are objected to because of the following informalities:

Regarding claim 22, the limitation "having a threshold voltage adjustment implant" is objected to. Claim 21 recites a halo implant. It is clear from the specification and drawings that the halo implant and the threshold voltage adjustment implant are the same thing. However, the claim as written appears to indicate that the two implants are distinct regions.

Regarding claim 26, the limitation "at a first of said reset transistor" should be changed to read "at a first side of said reset transistor".

Regarding claim 49, the limitation "by a portion of a substrate supporting said transistor" appears twice in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 7, 9, 14, 32-34, 37, 38, 41, 42, 45, 50, 85, 86, and 89 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuriyama et al. (US Pat. 6,166,405, hereinafter Kuriyama).

Regarding claims 1, 3, and 7, Figure 1 of Kuriyama discloses a photoconversion device 13 (photodiode) (col. 5, line 66 – col. 6, line 5); and a first transistor (charge transfer transistor) (col. 5, lines 20-24) associated with said photoconversion device at a first side (left side) of said first transistor, said first transistor having a single active area extension region 14b on a second side (right side) of said transistor opposite said first side.

Regarding claims 1 and 2, Figure 5 of Kuriyama discloses a photoconversion device 33; and a first transistor (reset transfer transistor) (col. 11, lines 18-21) associated with said photoconversion device at a first side (left side) of said first transistor, said first transistor having a single active area extension region 34b on a second side (right side) of said transistor opposite said first side.

Regarding claim 9, Figure 1 of Kuriyama discloses said photoconversion device 13 is part of a four transistor pixel circuit comprising a transfer transistor as said first transistor (col. 5, lines 20-24), a reset transistor, a source follower transistor (amplification FET), and a row select transistor (select FET).

Regarding claim 14, Figure 3 of Kuriyama discloses said first transistor has a single insulating spacer, said spacer positioned on said second side (right side) of said transistor.

Regarding claims 32 and 37, Figures 1 and 5 of Kuriyama discloses a pixel array (col. 2, lines 24-26), at least one pixel of said array comprising: a photoconversion device 13/33 (photodiode) (col. 5, line 66 – col. 6, line 5), and a first transistor gate 12/32 associated with said photoconversion device at a first side (left side) of said transistor gate, said transistor gate having a single lightly doped drain 14b/34b on a second side (right side) of said transistor gate opposite said first side. It is inherent that the pixel array of Kuriyama supplies signals to some type of image processor.

Regarding claim 33, Figure 5 of Kuriyama discloses said first transistor gate 32 is of a reset transistor (col. 11, lines 18-21) in electrical communication with said photoconversion device 33.

Regarding claim 34, Figure 1 of Kuriyama discloses said first transistor gate 12 is of a transfer transistor (col. 5, lines 20-24) in electrical communication with said photoconversion device 13.

Regarding claims 38, Figure 1 of Kuriyama discloses a semiconductor transistor (charge transfer transistor) (col. 5, lines 20-24) in contact with a photodiode 13 (col. 5, line 66 – col. 6,

line 5) comprising a single active area extension 14b on a side of said transistor opposite from said photodiode.

Regarding claim 41, Figure 1 of Kuriyama discloses a source/drain region 14a and said active area extension region 14b are spaced away from a gate 12 of said first transistor by a portion 11 of a substrate 10/11 supporting said first transistor. Note that insulating film 11 can be considered to be part of the substrate.

Regarding claim 42, Figure 1 of Kuriyama discloses an insulating layer 15a/b over said transistor and said photodiode, said insulating layer extending to a floating diffusion region 14a adjacent to said active area extension region.

Regarding claim 45, Figure 1 of Kuriyama discloses said transistor (charge transfer transistor) (col. 5, lines 20-24) is part of a pixel having at least two other transistors (reset and select transistors) in electrical communication with said photodiode 13.

Regarding claim 50, Figure 1 of Kuriyama discloses a semiconductor transistor (charge transfer transistor) (col. 5, lines 20-24) in electrical contact with a photodiode 13 (col. 5, line 66 – col. 6, line 5), said transistor comprising a single active area extension region 14b on a opposite side of said transistor from said photodiode and a source/drain region adjacent to said active area extension region, said active area extension region and said source/drain region being spaced away from a gate 12 of said transistor. Note that region 14b is spaced from the gate by the insulating film 11.

Regarding claim 85, Figure 1 of Kuriyama discloses a semiconductor transistor (charge transfer transistor) (col. 5, lines 20-24) comprising a channel region between a higher voltage side (right side) and a lower voltage side (left side), and a single active area extension region 14b

at said higher voltage side of said channel, said transistor being associated with circuitry of a photoimaging circuit. Note that it is inherent that the side (left side) with the photoconversion element 13 has a lower voltage than the side (right side) connected to the power source.

Regarding claim 86, Kuriyama discloses the transistor is part of a pixel (col. 5, lines 18-21).

Regarding claim 89, Figure 1 of Kuriyama discloses the transistor is associated with a photodiode 13 (col. 5, line 66 – col. 6, line 5) of a CMOS imager pixel.

Claims 1, 5, 38, 40, 46, 47, 85, and 87 are rejected under 35 U.S.C. 102(e) as being anticipated by Stevens et al. (US Pat. 6,730,899, hereinafter Stevens).

Regarding claims 1 and 38, Figures 2 and 3 of Stevens disclose a photoconversion device PD; and a first semiconductor transistor TG associated with (in electrical contact with) said photoconversion device at a first side of said first transistor, said first transistor having a single active area extension region 80 on a second side of said transistor opposite said first side.

Regarding claims 5 and 40, Figure 2 of Stevens discloses said first transistor TG has a gate length which is increased relative to other transistors (RG and unlabeled transistor to the right of transistor 100). Note that the instant application defines the gate length as the distance labeled 44 in Figure 1(a) (see paragraph[0033]). It is clear that the corresponding feature in Figures 2 and 3 of Guidash is larger in the first transistor TG than in the other two transistors indicated above.

Regarding claim 46, Figures 2 and 3 of Stevens disclose a semiconductor transistor TG in electrical contact with a photodiode PD, said transistor having a gate length which is increased

relative to any other transistor (RG) gate length of transistors of a same pixel. Regarding the gate length, see the discussion of claim 5 above.

Regarding claim 47, Figure 3 of Stevens discloses a single active area extension region 80 on an opposite side of said transistor from said photodiode PD.

Regarding claim 85, Figures 3 of Stevens discloses a semiconductor transistor TG comprising a channel region between a higher voltage side (right side) and a lower voltage side (left side), and a single active area extension region 80 at said higher voltage side of said channel, said transistor being associated with circuitry of a photoimaging circuit. Note that it is inherent that the side (left side) with the photoconversion element 69 has a lower voltage than the side (right side) connected to the output circuitry.

Regarding claim 87, Figure 2 of Stevens discloses said transistor TG has a gate length which is increased relative to any transistor gate length of other transistors (RG) of a same photoimager circuit. Regarding the gate length, see the discussion of claim 5 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama.

Regarding claim 10, Kuriyama does not explicitly disclose that at least one of said reset transistor and said source follower transistor (amplification FET) have a single active area extension region. However, as stated above, Figure 1 of Kuriyama discloses a single active area extension region 14b for the transfer transistor. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including an active area extension region (LDD region) in at least one of the reset FET and the amplification FET for the purpose of inhibiting short channel effects and hot carrier generation in those transistors as well as the transfer transistor. Employing an LDD region for the above stated purpose is extremely well known in the art.

Regarding claim 13, the difference between Kuriyama and the claimed invention is said active area extension region said first transistor has a dopant concentration of about 1×10^{12} to about 3×10^{13} ions/cm^3. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Kuriyama by using the claimed range of dopant concentration, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claims 4, 6, 8, 21, 22, 24-30, 35, 39, 43, 51, and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama in view of Komuro (US Pat. 5,780,902).

Regarding claims 4, 6, 35, 39, 51, and 88, the difference between Kuriyama and the claimed invention is the channel region of said first transistor has a threshold voltage adjustment implant (halo implant region) extending partially below a gate of said first transistor. Figure 5C

of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed in the channel (below an LDD region) and partially under the gate electrode. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro).

Regarding claim 8, Figure 1 of Kuriyama discloses said single active area extension region 14b is spaced away from a gate 12 of said first transistor by a portion 11 of a substrate 10/11 supporting said first transistor. Note that insulating film 11 can be considered to be part of the substrate. Therefore, both the active area extension region and the halo implant will be spaced from the gate by a portion of the substrate.

Regarding claims 21, 22, and 25, Figure 5 of Kuriyama discloses a semiconductor substrate 30, a reset transistor (col. 11, lines 19-21) over said substrate; a photosensor 33 in electrical communication with said reset transistor, said photosensor being within said substrate on a first side of said reset transistor; and a single active area extension region (lightly-doped drain (LDD)) 34b in said substrate adjacent to said reset transistor, said single active area extension region being on a side of said reset transistor which is opposite to said first side. The difference between Kuriyama and the claimed invention is a halo implant region in said substrate below said single active area extension region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed in the channel region (in the substrate 1) and below an LDD region. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a

halo implant region for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro).

Regarding claim 24, Figure 5 of Kuriyama discloses said photosensor 33 and said reset transistor are part of a transistor pixel circuit that further comprises a source follower transistor (amplification FET) and a row select transistor (select FET).

Regarding claim 26, Figure 5 of Kuriyama discloses a semiconductor substrate 30; a reset transistor (col. 11, lines 19-21) over said substrate; a floating diffusion region 34a in said substrate and in electrical communication with said reset transistor at a first side of said reset transistor; and a single active area extension region 34b in said substrate adjacent to said reset transistor, said single active area extension region being on a second side of said reset transistor which is opposite to said first side. The difference between Kuriyama and the claimed invention is a halo implant region in said substrate below said single active area extension region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed in the channel region (in the substrate 1) and below an LDD region. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro).

Regarding claims 27 and 43, the disclosure of Kuriyama does not explicitly disclose the image sensor is a CMOS imager. However, it would have been obvious to the ordinary artisan at the time the invention was made to use a CMOS imager as disclosed in the background of Kuriyama (col. 1, lines 18-25) for the purpose of integrating input elements with peripheral circuits on one chip.

Regarding claim 28, Figure 5 of Kuriyama discloses a photodiode 33 (col. 11, lines 64-66) in electrical contact with said reset transistor, said photodiode being within said substrate on said first side of said reset transistor.

Regarding claims 29 and 30, Kuriyama discloses an imaging device with an array of pixels (col. 2, lines 24-26). It can be considered that "a sensor array" includes all elements of each pixel (e.g., photosensors, transistors, diffusion regions). Therefore, the floating diffusion region is located within the sensor array. Alternatively, it can be considered that "a sensor array" only includes the photosensor portions of each pixel. In this case, the floating diffusion region is located outside the sensor array.

Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama in view of Park et al. (US Pat. 6,794,215, hereinafter Park).

Regarding claim 15, Figure 1 of Kuriyama discloses a semiconductor substrate 10; a transfer transistor (col. 5, lines 20-24) over said substrate, said transfer transistor having a single active area extension region 14b located on a first side (right side) of said transfer transistor; a photosensor 13 in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side; a reset transistor gate; and a floating diffusion region 14a on the first side of said transfer transistor and adjacent said reset transistor gate, said floating diffusion region in electrical communication with said active area extension region. Kuriyama does not explicitly disclose that the reset transistor gate is over said substrate and spaced apart from said transfer transistor. Figure 1 of Park discloses a CMOS image sensor with both a transfer transistor Tx and a reset

transistor Rx spaced apart from each other and on a substrate 11. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including the reset transistor on the substrate for the purpose of increasing the integration density.

Regarding claim 20, Figure 1 of Kuriyama discloses a row select transistor (select FET).

Claims 16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama in view of Park as applied to claim 15 above, and further in view of Komuro.

Regarding claim 16, a further difference between Kuriyama and the claimed invention is the channel region of said transfer transistor having a threshold voltage adjustment implant (halo implant). Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed in the channel region (in the substrate 1) and below an LDD region. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro).

Regarding claims 18 and 19, a further difference between Kuriyama and the claimed invention is said reset transistor comprises two active area extension regions as lightly doped drains on opposite sides of said reset transistor. Figure 5C of Komuro discloses LDD regions 5 on opposite sides of a MOS transistor. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including LDD regions on opposite sides of the reset transistor for the purpose of suppressing

short channel effects and hot carrier generation, which is well known in the art. Note that a device having active area extension regions on both sides still reads on the limitation "a single active area extension region on a side opposite said floating diffusion region", since there is a single extension region on the opposite side. In other words, the opposite does not have more than one extension region.

Claims 15, 17, 32, 36, 47, 49, 50, and 52 rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens in view of Kuriyama.

Regarding claim 15, Figures 2 and 3 of Stevens disclose a semiconductor substrate 73; a transfer transistor TG over said substrate; a photosensor PD in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side; a reset transistor gate RG over said substrate and spaced apart from said transfer transistor; and a floating diffusion region 80 on the first side of said transfer transistor and adjacent said reset transistor gate. The difference between Stevens and the claimed invention is said transfer transistor having a single active area extension region located on a first side of said transfer transistor. Figure 1 of Kuriyama discloses a single active area extension region 14b (LDD region) on one side of a transfer transistor and a photodiode 13 (col. 5, lines 65-67) on the opposite side. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens by including an active area extension region (LDD region) on the second side of the

first transistor for the purpose of suppressing deterioration of the element properties (col. 6, lines 16-18 of Kuriyama).

Regarding claims 17, 36, and 52, Figure 2 of Stevens discloses said first transistor TG has a gate length which is increased relative to other transistors (RG and unlabeled transistor to the right of transistor 100). Note that the instant application defines the gate length as the distance labeled 44 in Figure 1(a) (see paragraph[0033]). It is clear that the corresponding feature in Figures 2 and 3 of Guidash is larger in the first transistor TG than in the other two transistors indicated above.

Regarding claim 32, Figures 2 and 3 of Stevens disclose a pixel array, at least one pixel of said array comprising: a photoconversion device PD, and a first transistor gate 76 associated with said photoconversion device at a first side of said transistor gate. It is inherent that the pixel array of Kuriyama supplies signals to some type of image processor. The difference between Stevens and the claimed invention is said transistor gate having a single lightly doped drain on a second side of said transistor gate opposite said first side. Figure 1 of Kuriyama discloses a single active area extension region 14b (LDD region) on one side of a transfer transistor and a photodiode 13 (col. 5, lines 65-67) on the opposite side. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens by including an active area extension region (LDD region) on the second side of the first transistor for the purpose of suppressing deterioration of the element properties (col. 6, lines 16-18 of Kuriyama).

Regarding claims 47 and 49, Figures 2 and 3 of Stevens disclose a source/drain region 80. The difference between Stevens and the claimed invention is a single active area extension

region adjacent the source/drain region. Figure 1 of Kuriyama discloses a single active area extension region 14b (LDD region) adjacent a source/drain region 14a on one side of a transfer transistor and a photodiode 13 (col. 5, lines 65-67) on the opposite side. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens by including an active area extension region (LDD region) adjacent the source/drain region for the purpose of suppressing deterioration of the element properties (col. 6, lines 16-18 of Kuriyama). Note that both the active area extension region and the source/drain region will be spaced away from the gate 76 by a portion 74 of a substrate 73/74 (Figure 3 of Stevens). Note that insulating film 74 can be considered to be part of the substrate.

Regarding claim 50, Figures 2 and 3 of Stevens disclose a semiconductor transistor TG in electrical contact with a photodiode PD, said transistor comprising a source/drain region 80. The difference between Stevens and the claimed invention is a single active area extension region adjacent the source/drain region. Figure 1 of Kuriyama discloses a single active area extension region 14b (LDD region) adjacent a source/drain region 14a on one side of a transfer transistor and a photodiode 13 (col. 5, lines 65-67) on the opposite side. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens by including an active area extension region (LDD region) adjacent the source/drain region for the purpose of suppressing deterioration of the element properties (col. 6, lines 16-18 of Kuriyama). Note that both the active area extension region and the source/drain region will be spaced away from the gate 76 by insulating layer 74 (Figure 3 of Stevens).

Claim 48 rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens in view of Kuriyama as applied to claim 47 above, and further in view of Komuro.

A further difference between Stevens and the claimed invention is a threshold voltage adjustment implant (halo implant) below a gate of said transistor. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (pocket) 14 formed in the channel (below an LDD region) and partially under the gate electrode. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region for the purpose of suppressing short channel effects and also the hot carrier generation (see abstract of Komuro).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Tom Thomas

SUPERVISORY PATENT EXAMINER

Matthew C. Landau

Examiner

April 16, 2005